CLAIMS

What is claimed is:

1. A magnetic random access memory (MRAM) with stackable architecture comprising:

a first memory column comprising a plurality of magnetic memory cells electrically coupled and stacked on top of each other, each magnetic memory cell configured to store data;

a first conductive word line electrically coupled to the first memory column; and

a first bit line column horizontally disposed from and parallel to the first memory column, the first bit line column electrically isolated from the first word line and comprising a plurality of conductive bit lines electrically isolated from the first memory column and from each other, the first bit line column positioned close enough such that an electric current passing through one of the plurality of bit lines will produce a magnetic field affecting one of the plurality of magnetic memory cells.

2. The MRAM of claim 1 wherein one of each of the plurality of bit lines is vertically aligned with one of each of the plurality of magnetic memory cells.

3. The MRAM of claim 1 wherein each of the plurality of bit lines is perpendicular to the first memory column.

4. The MRAM of claim 1 further comprising:

an insulator positioned between the bit line column and the memory column..

5. The MRAM of claim 1, further comprising:

a second bit line column electrically isolated from the first word line, the second bit line column comprising a plurality of conductive bit lines electrically isolated from each other and configured to carry electric current during a memory read and a memory write.

6. The MRAM of claim 5 wherein the second bit line column is electrically isolated from the first memory column.

7. The MRAM of claim 6 wherein the second bit line column is parallel to the first bit line column.

8. The MRAM of claim 7 wherein the first and second bit line columns are perpendicular to the first word line.

9. The MRAM of claim 7 wherein the first and second bit line columns are on opposite sides of the first memory column.

10. The MRAM of claim 9 further comprising:

a second memory column electrically coupled to the first word line and comprising a plurality of magnetic memory cells electrically coupled and adjacent to each other, each memory cell configured to store data, the second memory column parallel to the first memory column and adjacent to the first bit line column.

11. The MRAM of claim 10 further comprising:

a second conductive word line parallel to the first word line; and

a third memory column electrically coupled to the second word line and comprising a plurality of magnetic memory cells electrically coupled and adjacent to each other, each memory cell configured to store data.

12. The MRAM of claim 11 wherein the third memory column is parallel to the first memory column.

13. The MRAM of claim 12 wherein the third memory column is positioned between the first and second bit line columns.

14. The MRAM of claim 11 wherein one of the plurality of memory cells in the first memory column is configured to store data when electric current flows through the first word line into the first memory column and electric current flows through one of the plurality of bit lines in the second bit line column.

15. The MRAM of claim 14 wherein one of the plurality of memory cells in the first memory column is further configured to store data when electric current flows through one of the plurality of bit lines in the first bit line column.

16. The MRAM of claim 15 wherein the direction of current flowing through one of the plurality of bit lines in the first bit line column is opposite the direction of current flowing through one of the plurality of bit lines in the second bit line column.

17. The MRAM of claim 15 wherein the direction of current flowing through one of the plurality of bit lines in the first bit line column is the same as the direction of current flowing through one of the plurality of bit lines in the second bit line column.

18. The MRAM of claim 1, each of the plurality of memory cells in the first memory column further comprising:

a readout layer configured to have a magnetic polarization; and

a storage layer coupled to the readout layer and configured to have a magnetic polarization, the storage layer having a higher coercivity than the readout layer.

19. The MRAM of claim 18, wherein the readout layer and the storage layer are configured to align their magnetic polarizations with a magnetic field generated by the electric current in one of the plurality of bit lines during memory write, and the readout layer is configured to align its magnetic polarization with a magnetic field generated by the electric current in one of the plurality of bit lines during memory read.

20. A magnetic random access memory (MRAM) with stackable architecture comprising:

a word line configured to carry electric current;

a magnetic memory cell electrically coupled to the word line and configured to store data; and

a bit line magnetically coupled to the magnetic memory cell and electrically isolated from the word line, the bit line configured to set a magnetic polarization within the magnetic memory cell during a memory write operation and to set a

magnetic polarization within the magnetic memory cell during a memory read operation.

21. The MRAM of claim 20 wherein the bit line is further configured to reverse a magnetic polarization within the magnetic memory cell during the memory read operation.

22. A method of writing to magnetic random access memory (MRAM) with a word line, a magnetic memory cell electrically coupled to the word line, and a bit line magnetically coupled to, adjacent to and electrically isolated from the memory cell, the method comprising:

generating an electric current in the word line;

receiving an electric current in the magnetic memory cell;

generating a magnetic field around the bit line; and

aligning a magnetic polarization within the magnetic memory cell according to the direction of the magnetic field.

23. The method of claim 22 further comprising:

aligning a magnetic polarization within a readout layer in the magnetic memory cell according to the direction of the magnetic field; and

aligning a magnetic polarization within a storage layer according to the direction of the magnetic field, the storage layer coupled to the readout layer and having a higher coercivity than the readout layer.

24. The method of claim 23, further comprising:

generating an electric current; and

electrically lowering the switching field of the memory cell.

25. The method of claim 23, further comprising:

heating the memory cell; and

lowering the switching field of the memory cell.

26. The method of claim 23, further comprising:

generating an electric current; and

magnetically lowering the switching field of the memory cell.

27. A method of reading from a magnetic random access memory (MRAM) with a word line, a magnetic memory cell electrically coupled to the word line, and a bit line magnetically coupled to, adjacent to and electrically isolated from the magnetic memory cell, the method comprising:

generating a magnetic field around the bit line;

aligning a magnetic polarization within the memory cell according to the direction of the magnetic field;

measuring a resistance of the memory cell;

reversing the magnetic polarization within the magnetic memory cell; and

measuring the resistance of the magnetic memory cell.

28. The method of claim 27 further comprising:

generating an electric current in the word line; and

receiving an electric current in the magnetic memory cell.

29. The method of claim 27 further comprising:

reversing the magnetic field around the bit line.

30. The method of claim 27 further comprising:

aligning a magnetic polarization within a readout layer in the magnetic memory cell according to the direction of the magnetic field; and

reversing the magnetic polarization within the readout layer.

31. A method of reading from a magnetic random access memory (MRAM) with a word line, a magnetic memory cell electrically coupled to the word line, and a bit line magnetically coupled to, adjacent to and electrically isolated from the memory cell, the method comprising:

measuring the resistance of the magnetic memory cell;

generating a magnetic field around the bit line;

reversing a magnetically pre-existing polarization within the magnetic memory cell according to the direction of the magnetic field; and

measuring the resistance of the memory cell.

32. A method of selecting a magnetic random access memory (MRAM) with a word line, a plurality of magnetic memory cells forming a memory column and electrically coupled to the word line, a bit line magnetically coupled to, adjacent to and electrically isolated from the memory column, a switch coupled to the memory column, the method comprising:

generating an electric current in the word line; and

activating no more than the switch.

33. A magnetic random access memory (MRAM) with stackable architecture comprising:

a memory cell comprising:

a storage layer with high-coercivity configured for storing information;

a thin insulating layer coupled to the storage layer and configured to form a magnetic tunneling junction (MTJ); and

a readout layer with low-coercivity coupled to the thin insulating

layer and configured to provide a relative readout for determining the magnetization of the storage layer.

34. The MRAM of claim 33 wherein the storage and readout layers further comprise a plurality of CoPt layers, wherein the number of CoPt layers determines the relative coercivity between the storage and readout layers.

35. The MRAM of claim 34 further comprising:

a first bit line magnetically coupled to and electrically isolated from the magnetic memory cell; and

a second bit line magnetically coupled to and electrically isolated from the magnetic memory cell and parallel to the first bit line, wherein the first and second bit lines are configured to generate a magnetic field at the location of the magnetic memory cell by conveying electric current in opposite directions.

36. The MRAM of claim 34 further comprising:

a first bit line magnetically coupled to and electrically isolated from the magnetic memory cell; and

a second bit line magnetically coupled to and electrically isolated from the magnetic memory cell and parallel to the first bit line, wherein the first and second bit lines are configured to generate a magnetic field at the location of the magnetic memory cell by conveying electric current in the same direction.

37. The MRAM of claim 36 wherein the magnetic memory cell is between the first and second bit lines.

38. The MRAM of claim 36 further comprising:

a cladding layer coupled to the storage layer and configured to magnetically couple the first and second bit lines to the magnetic memory cell, wherein the magnetization of the storage layer switches through anti-parallel magnetic coupling of the storage layer and the cladding layer.

39. The MRAM of claim 38 further comprising:

a first CuTa layer coupled to the memory cell;

a second CuTa layer coupled to the first bit line; and

a third CuTa layer coupled to the second bit line, the first, second and third CuTa layers configured to control the resistance of the magnetic memory cell, first and second bit lines.

40. A magnetic random access memory (MRAM) with stackable layers, the MRAM having a plurality of conductive word lines, a first layer comprising:

a first plurality of magnetic memory cells aligned in a first row, each of the first plurality of memory cells separated by an insulator and electrically isolated from each other and configured to store information, each magnetic memory cell coupled to one of each of the plurality of word lines; and

a first conductive bit line parallel to, horizontally disposed from, and electrically isolated from the first row, the first bit line configured to select from the first plurality of magnetic memory cells, wherein the first bit line is close enough to be magnetically coupled to the first row.

41. The MRAM of claim 40, further comprising:

a second conductive bit line parallel to the first row, the first row positioned between the first and second bit lines and electrically isolated from the first row, the second bit line configured, in conjunction with the first bit line, to select from the

first plurality of magnetic memory cells, wherein the second bit line is close enough to be magnetically coupled to the first row.

42. The MRAM of claim 41 further comprising:

a second plurality of magnetic memory cells aligned in a second row, each of the second plurality of memory cells electrically isolated from each other and configured to store information, the second row parallel to and horizontally disposed from the first row, the second bit line positioned between the second row and the first row, each of the plurality of word lines coupled to one of each of the first and second plurality of magnetic memory cells.

43. The MRAM of claim 42 wherein the first and second bit lines and the first and second rows are vertically aligned with each other.

44. The MRAM of claim 42, a second layer comprising:

a third plurality of magnetic memory cells aligned in a third row, each of the third plurality of memory cells electrically isolated from each other and configured to store information, each of the third plurality of magnetic memory cells

electrically coupled to one of each of the first plurality of magnetic memory cells, the third row vertically disposed and beneath the first row; and

a conductive third bit line parallel to, horizontally disposed from, and electrically isolated from the third row, the third bit line configured to select from the third plurality of magnetic memory cells, wherein the third bit line is close enough to be magnetically coupled to the third row, the third bit line vertically disposed and beneath the first bit line.

45. The MRAM of claim 44, further comprising:

a conductive fourth bit line parallel to the third row, the third row of magnetic memory cells positioned between the third and fourth bit lines, the fourth bit line configured, in conjunction with the second bit line, to select from the third plurality of magnetic memory cells, wherein the fourth bit line is close enough to be magnetically coupled to the first row.

46. The MRAM of claim 45 further comprising:

a second plurality of magnetic memory cells aligned in a second row, each memory cell in the second row electrically isolated from every other memory cell in the second row and configured to store information, the second row parallel to and

horizontally disposed from the first row, the second bit line positioned between the second row and the first row, each of the plurality of word lines coupled to one of each of the first and second plurality of magnetic memory cells.

47. A method of manufacturing a co-planar magnetic random access memory cell (MRAM), comprising:

depositing a plurality of magnetic memory cells on a dielectric surface; and

depositing a plurality of bit lines on a dielectric surface simultaneously with the depositing of the plurality of memory cells.